Attorney's Docket No. 5308-156 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Ryu et al.
Serial No.: To Be Assigned
Filed: Concurrently herewith
For: SILICON CARBIDE POWER METAL-OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTORS HAVING A SHORTING CHANNEL AND METHODS OF FABRICATING SILICON CARBIDE METAL-OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTORS HAVING A SHORTING CHANNEL

Date: July 26, 2001

BOX PATENT APPLICATION
Commissioner for Patents
Washington, DC 20231

PRELIMINARY AMENDMENT

Sir:

Please make the following amendments to the present application prior to examination and prior to calculation of any fees. Applicants provide attached hereto an appendix entitled "VERSION WITH MARKINGS SHOWING CHANGES" showing the changes made by the present Preliminary Amendment.

In the Specification:

Please replace the paragraph beginning at Page 18, line 27 with the following paragraph:

Figure 8F illustrates the formation and patterning of the gate oxide **28**. The gate oxide is preferably thermally grown and is a nitrided oxide. The nitrided oxide may be any suitable gate oxide, however, SiO_2, oxynitride or ONO may be preferred. Formation of the gate oxide or the initial oxide of an ONO gate dielectric is preferably followed by an anneal in N_2O or NO so as to reduce defect density at the SiC/oxide interface. In particular embodiments, the gate oxide is formed either by thermal growth or deposition and then annealed in an N_2O environment at a temperature of greater than about 1100 °C and flow rates of from about 2 to about 8 SLM which may provide initial residence times of the N_2O of from about 11 to about 45 seconds. Such formation and annealing of an oxide layer on silicon carbide are described in commonly assigned United States Patent Application Serial No. 09/834,283, entitled "Method of N_2O Annealing an Oxide Layer on a Silicon Carbide Layer" (Attorney Docket No. 5308-157) or as described in United States Provisional Application Serial

No. 60/294,307 entitled "Method of N_2O Growth of an oxide layer on a Silicon Carbide Layer" filed May 30, 2001, the disclosures of which are incorporated herein by reference as if set forth fully herein. Additionally, an N_2O grown oxide may also be utilized as described in J. P. Xu, P. T. Lai, C. L. Chan, B. Li, and Y. C. Cheng, "Improved Performance and Reliability of N_2O-Grown Oxynitride on 6H-SiC," IEEE Electron Device Letters, Vol. 21, No. 6, pp. 298-300, June 2000. Techniques as described in L. A. Lipkin and J. W. Palmour, "Low interface state density oxides on p-type SiC," Materials Science Forum Vols. 264-268, pp. 853-856, 1998 may also be utilized. Alternatively, for thermally grown oxides, a subsequent NO anneal of the thermally grown SiO_2 layer may be provided to reduce the interface trap density as is described in M. K. Das, L. A. Lipkin, J. W. Palmour, G. Y. Chung, J. R. Williams, K. McDonald, and L. C. Feldman, "High Mobility 4H-SiC Inversion Mode MOSFETs Using Thermally Grown, NO Annealed SiO_2," IEEE Device Research Conference, Denver, CO, June 19-21, 2000; G. Y. Chung, C. C. Tin, J. R. Williams, K. McDonald, R. A. Weller, S. T. Pantelides, L. C. Feldman, M. K. Das, and J. W. Palmour, "Improved Inversion Channel Mobility for 4H-SiC MOSFETs Following High Temperature Anneals in Nitric Oxide," IEEE Electron Device Letters accepted for publication; and G. Y. Chung, C. C. Tin, J. R. Williams, K. McDonald, M. Di Ventra, S. T. Pantelides, L. C. Feldman, and R. A. Weller, "Effect of nitric oxide annealing on the interface trap densities near the band edges in the 4H polytype of silicon carbide," Applied Physics Letters, Vol. 76, No. 13, pp. 1713-1715, March 2000. Oxynitrides may be provided as described in United States Patent Application Serial No. 09/878,442, entitled "High Voltage, High Temperature Capacitor Structures and Methods of Fabrication" filed June 11, 2001, the disclosure of which is incorporated herein by reference as if set forth fully herein.

In the Claims:

Please cancel the second occurrence of Claim 66 on page 53 at line 24.

Please add the following Claim 90:

90. (New) The method of Claim 61, wherein the third mask is patterned so that the second regions of n-type silicon carbide extend a distance of from about 0.5 μm to about 5 μm from the first regions of n-type silicon carbide to the peripheries of the first regions of p-type silicon carbide.

REMARKS

Applicants provide the present Preliminary Amendment to insert serial numbers of applications referred to in the specification and to correct a double numbering of Claim 66. Applicants have eliminated the two Claims 66 by canceling the second occurrence of Claim 66 on page 35 of the specification and adding new Claim 90 which corresponds to the canceled second occurrence of Claim 66.

Respectfully submitted,

Timothy J. O'Sullivan
Registration No. 35,632

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20792
PATENT TRADEMARK OFFICE

CERTIFICATE OF EXPRESS MAILING

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I hereby certify that this correspondence is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to Box Patent Application, Commissioner For Patents, Washington, DC 20231.

Traci A. Brown
Date of Signature: July 24, 2001
204953

VERSION WITH MARKINGS SHOWING CHANGES

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